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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/739,580	12/15/2000	Steven Teig	SPLX.P0015	3527
23349	7590	07/12/2004	EXAMINER GARBOWSKI, LEIGH M	
STATTLER JOHANSEN & ADELI P O BOX 51860 PALO ALTO, CA 94303			ART UNIT 2825	PAPER NUMBER

DATE MAILED: 07/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/739,580

Applicant(s)

TEIG ET AL.

Examiner

Leigh Marie Garbowski

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 28-45 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 28-45 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 09 July 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. ____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____. |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date (<u>14 sheets</u>). | 6) <input type="checkbox"/> Other: ____. |

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 28-37 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 15-23 of U.S. Patent No. 6,687,893 B2. Although the conflicting claims are not identical, they are not patentably distinct from each other because the subject matter claimed in the instant application is fully disclosed in the patent and is covered by the patent since the patent and the application are claiming common subject matter, as follows: taking claim 28, "for each combination of slots" is equivalent to line 53 of column 74, steps "a)" and "b)" are equivalent to lines 53-60; step "c)" is equivalent to lines 66-67 of column 74 and lines 2-3, 5, 14-15 of column 75 and lines 2-3, 5-6 of column 76; and step "d)" accordingly has equivalence with lines 62 of column 74 and lines 1-3 of column 75 and lines 1-3 of column 76. The remaining claims follow similarly.

Claim Objections

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Claims 41 and 43 are objected to because of the following informalities: taking claim 41 as exemplary, the use of "a)" in line 2 is confusing since claim 38 from which it depends already uses "a)" in line 5. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 36-37 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 36 recites the limitation "the first attribute" in line 2. There is insufficient antecedent basis for this limitation in the claim. Claim 37 is rejected based on its dependency.

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 38-45 are rejected under 35 U.S.C. 102(b) as being anticipated by Rostoker et al. [U.S. Patent #5,822,214].

As per claim 38, Rostoker et al. disclose a method comprising: a) selecting a first wiring model from among a plurality of wiring models, each model specifying different

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types of interconnect lines [column 58, line 36-column 59, line 63]; b) partitioning the IC regions into several sub-regions [column 42, lines 8-25]; c) selecting a net [column 58, lines 44-47]; d) identifying the set of sub-regions containing the circuit elements of the selected net [column 42, lines 48-58; column 56, line 56-column 62, line 13]; e) retrieving, from a storage structure, a pre-computed attribute of a set of one or more interconnect lines that are necessary for connecting the identified set of sub-regions, wherein said set of interconnect lines are based on the first wiring model [column 59, lines 5-63]. As per claim 39, wherein the retrieved attribute represents the placement cost of said net within said region [column 60, line 18-column 61, line 36]. As per claim 40, further comprising computing the placement cost of said net from said retrieved attribute [column 59, line 5-column 61, line 36]. As per claim 41, further comprising: changing the position of a circuit element of the net from one sub-region to another; identifying a new set of sub-regions that contain the circuit elements of the net; retrieving, from the storage structure, a pre-computed attribute of a different set of interconnect lines necessary for connecting the identified new set of sub-regions, wherein said different set of interconnect lines are based on the first wiring model [column 60, line 11-column 61, line 36].

As per claim 42, Rostoker et al. disclose a method comprising: a) selecting a first wiring model from among a plurality of wiring models, each model specifying different types of interconnect lines [column 58, line 36-column 59, line 63]; b) partitioning the IC regions into several sub-regions [column 42, lines 8-25]; c) for each particular net, identifying the set of sub-regions containing the circuit elements of the particular net

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[column 42, lines 48-58; column 56, line 56-column 62, line 13]; d) for each particular net, retrieving a pre-computed attribute of a connection graph that is based on the first wiring model and that represents the topology of interconnect lines needed to connect the identified set of sub-regions of the particular net [column 59, lines 5-63]; e) computing a placement cost for the IC layout within said region by using the retrieved attributes [column 59, line 5-column 61, line 36]. As per claim 43, further comprising: changing the position of a particular circuit element from one sub-region to another; for each particular net that includes the particular element, identifying a new set of sub-regions that contain the circuit elements of the particular net; for each particular net that includes the particular circuit element, retrieving a pre-computed attribute of a new connection graph that is based on the first wiring model, and that represents the topology of the interconnect lines necessary for connecting the identified new set of sub-regions for the particular net, [column 60, line 11-column 61, line 36]; computing a placement cost based on the retrieved attributes of the new connection graphs [column 59, line 5-column 61, line 36]. As per claims 44-45, wherein the connection graphs are Steiner trees and minimum spanning trees [column 59, lines 60-63].

Claims 38-43 are rejected under 35 U.S.C. 102(e) as being anticipated by Kanazawa [U.S. Patent #6,327,694 B1].

As per claim 38, Kanazawa discloses a method comprising: a) selecting a first wiring model from among a plurality of wiring models, each wiring model specifying different types of interconnect lines [column 14, lines 40-44]; b) partitioning the IC region into several sub-regions [column 14, lines 60-63]; c) selecting a net [column 14, lines

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54-60]; d) identifying the set of sub-regions containing the circuit elements of the selected net [column 14, line 65-column 15, line 1]; e) retrieving, from a storage structure, a pre-computed attribute of a set of one or more interconnect lines that are necessary for connecting the identified set of sub-regions, wherein said set of interconnect lines are based on the first wiring model [column 12, lines 59-61; column 15, lines 7-9]. As per claim 39, wherein the retrieved attribute represents the placement cost of said net within said region [column 10, lines 43-45]. As per claim 40, further comprising computing the placement cost of said net from said retrieved attribute [column 10, lines 43-45]. As per claim 41, further comprising: changing the position of a circuit element of the net from one sub-region to another; identifying a new set of sub-regions that contain the circuit elements of the net; retrieving, from the storage structure, a pre-computed attribute of a different set of interconnect lines necessary for connecting the identified new set of sub-regions, wherein said different set of interconnect lines are based on the first wiring model [column 10, lines 43-45; column 12, lines 59-61; column 14, line 65-column 15, line 9].

As per claim 42, Kanazawa discloses a method comprising: a) selecting a first wiring model from among a plurality of wiring models, each model specifying different types of interconnect lines [column 14, lines 40-44]; b) partitioning the IC regions into several sub-regions [column 14, lines 60-63]; c) for each particular net, identifying the set of sub-regions containing the circuit elements of the particular net [column 14, line 54- column 15, line 1]; d) for each particular net, retrieving a pre-computed attribute of a connection graph that is based on the first wiring model and that represents the

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topology of interconnect lines needed to connect the identified set of sub-regions of the particular net [column 12, lines 59-61; column 15, lines 7-9]; e) computing a placement cost for the IC layout within said region by using the retrieved attributes [column 10, lines 43-45]. As per claim 43, further comprising: changing the position of a particular circuit element from one sub-region to another; for each particular net that includes the particular element, identifying a new set of sub-regions that contain the circuit elements of the particular net; for each particular net that includes the particular circuit element, retrieving a pre-computed attribute of a new connection graph that is based on the first wiring model, and that represents the topology of the interconnect lines necessary for connecting the identified new set of sub-regions for the particular net; computing a placement cost based on the retrieved attributes of the new connection graphs [column 10, lines 43-45; column 12, lines 59-61; column 14, line 65-column 15, line 9].

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Igarashi et al. [U.S. Patent #5,224,057] disclose the importance of selecting a wiring model. Finery [U.S. Patent #5,251,147] disclose recursive graph partitioning. Sayah et al. [U.S. Patent #5,533,148] disclose recursive partitioning using a cost function. Hendrickson et al. [U.S. Patent #5,587,922] disclose graph partitioning. Kawaguchi [U.S. Patent #5,926,632] discloses circuit partitioning including evaluating the number of edges in a graph. Scepanovic et al. [U.S. Patent #6,067,409] disclose subdividing a circuit region and placing with a cost function.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leigh Marie Garbowski whose telephone number is 571-272-1893. The examiner can normally be reached on days.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



**LEIGH M. GARBOWSKI
PRIMARY EXAMINER**